

Figure 1

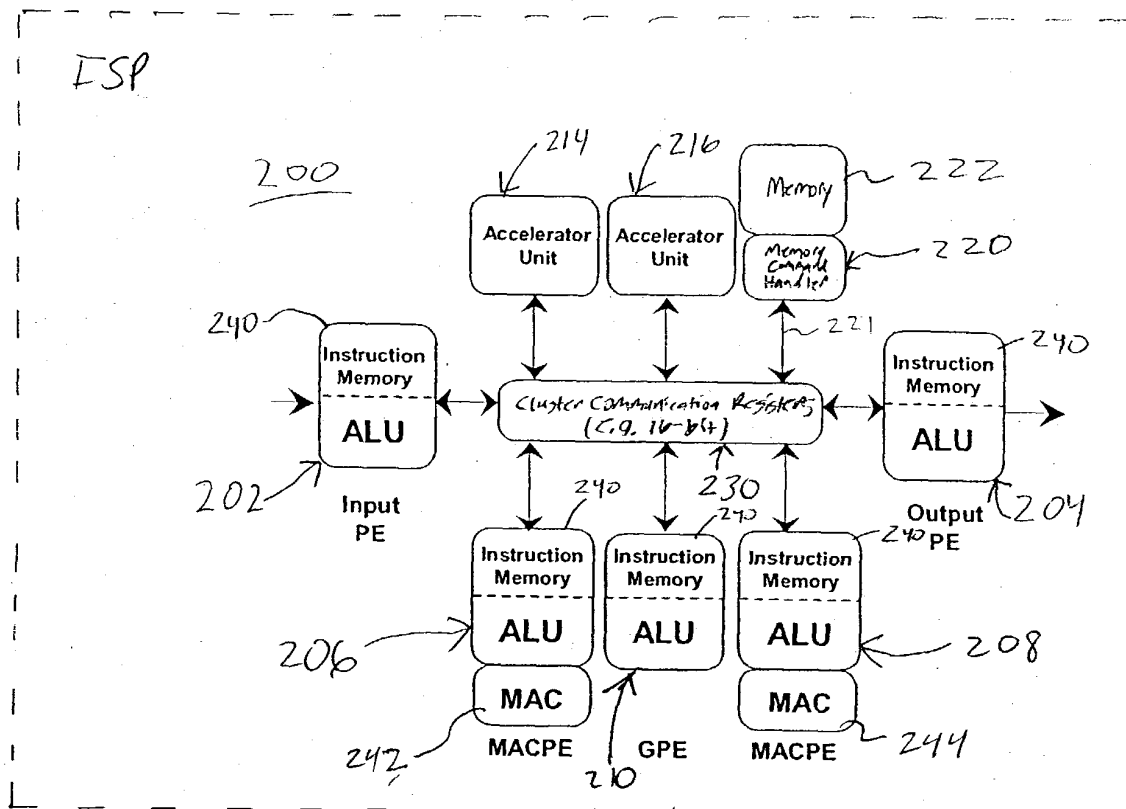


Figure 2

300

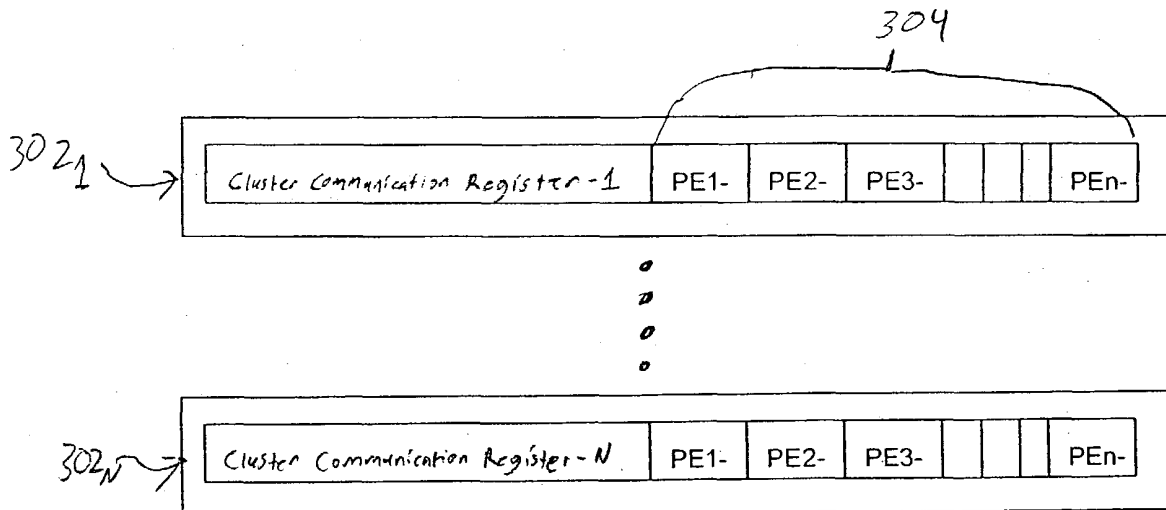


Figure 3

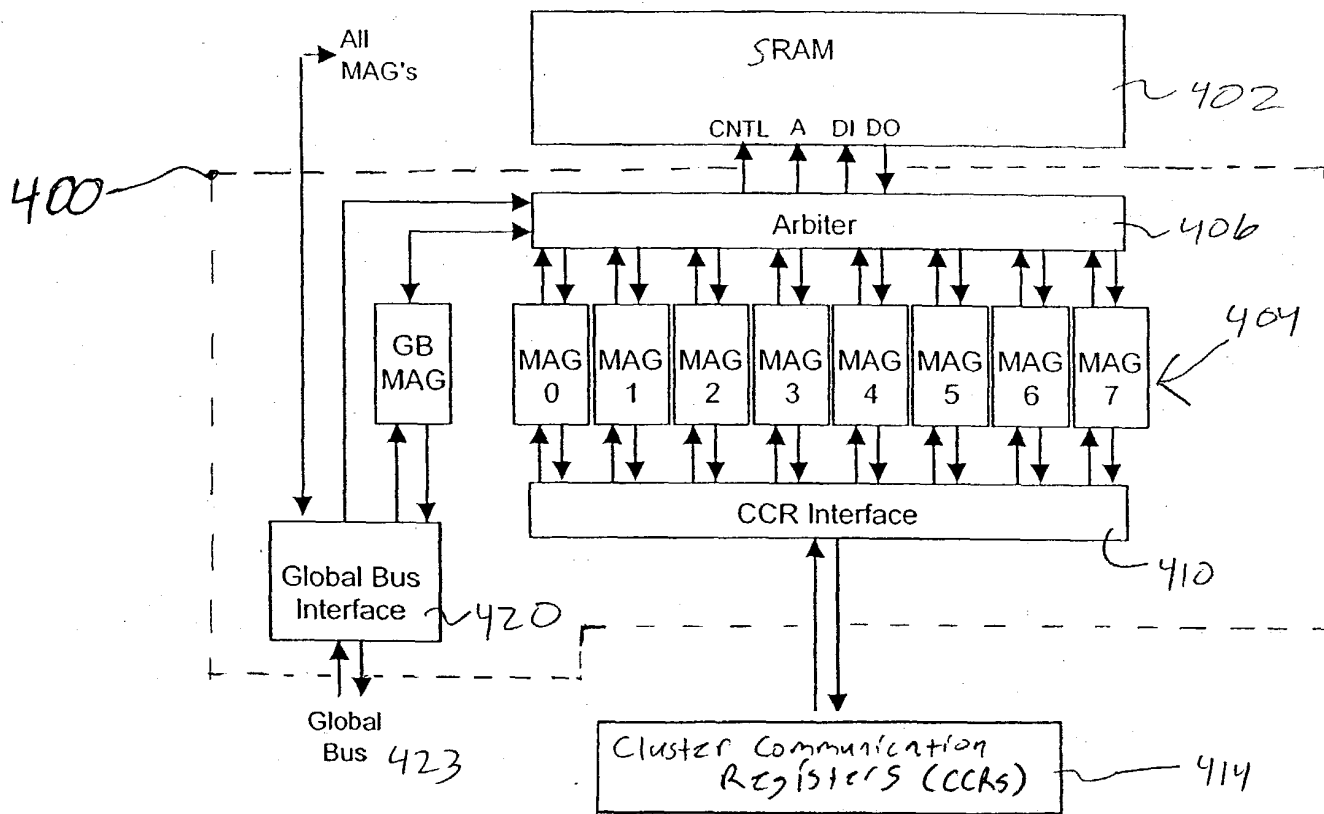


Figure 4

500

	MAG	MAG0	MAG1	MAG2	MAG3	MAG4	MAG5	MAG6	MAG7
502	CCR0	Command							
504	CCR1	Data							
506	CCR2		Command						
508	CCR3		Data						
510	CCR4			Command					
512	CCR5			Data					
:	CCR6				Command				
	CCR7				Data				
	CCR8					Command			
	CCR9					Data			
	CCR10						Command		
	CCR11						Data		
	CCR12							Command	
	CCR13							Data	
	CCR14								Command
	CCR15								Data

Figure 5

600

MAG

Mask Register	~ 602
Data Path DV Bits Register	~ 604
Base Offset Register	~ 606
Memory Pointer Register	~ 608
Increment Register	~ 610
Increment Register	~ 612
Operation Complete Register	~ 614
Control Bits	} 614
Control Bits	
o o * o o	

Figure 6

700

	MCH Command	Description
702	Write Mask	Used in address calculations to create circular buffer addressing
704	Set Data Path DV bits	Determines the target PE(s) for the read data
706	Read Immediate	Reads RAM from a specified address
708	Write Immediate	Writes RAM from the Data CCR to a specified RAM address
710	Write MPR	An initial offset value to be used in address calculations
712	Write Increment Register	Provides X and Y increment values for one or 2D addressing
714	Write Base Offset Register	Sets the Base Offset Register used in addressing
716	Read Indirect, N Words	Reads N words into the Data CCR using the MAG Memory Pointer
718	Write Indirect, N Words	Writes N words from the Data CCR using the MAG Memory Pointer
720	Read Op Complete	Used to signal the MCH control PE that a block transfer is complete
722	Infinite Indirect Operation	Set infinite indirect MCH operation

Figure 7

800

02 —

15	14	13	12	11	10	9	8-0	
0	0	x	x	x	x	x	x	Read Immediate
1	0	x	x	x	x	x	x	Write Immediate
0	1	0	x	x	x	x	x	Read Indirect
0	1	1	x	x	x	x	x	Write Indirect
1	1	0	1	x	x	x	x	Write Increment Registers
1	1	0	0	0	x	x	x	Set Data Path
1	1	0	0	1	0	0	x	Set Read Operation Complete
1	1	1	0	0	x	x	x	Write Memory Pointer Register
1	1	1	0	1	x	x	x	Write Base Offset
1	1	1	1	0	x	x	x	Write Mask Register
1	1	1	1	1	x	x	x	Write First Use Registers

Figure 8